B. The Smirnov Class $N^+$

The reader is referred to [5] for a full account of the Smirnov class $N^+$ and the Nevanlinna class $N$. We note that the proper inclusions $H^p \subset N^+ \subset N \subset C$ are valid.

The following theorem is a generalization of Theorem 1; the proof of Theorem 3 is found in [5].

Theorem 3: Every $r \times m$ matrix function $H(z)$ of class $N^+$ with rank $H(e^{j\omega}) = m$ a.e. can be expressed in the form

$$H(z) = H_0(z)H_1(z)$$

(20)

where $H_0(z)$ is inner, and $H_1(z)$ is any column outer function whose boundary value $H_1(e^{j\omega})$ satisfies the same magnitude-squared specification as $H(e^{j\omega})$. Moreover, the factorization (20) is unique up to multiplication by a constant unitary matrix.

By using Theorem 3 and the Parseval identity, we obtain the following theorem, which is a generalization of Theorem 2.

Theorem 4: Let $H(z)$ be an $r \times m$ matrix function of class $N^+$ with rank $H(e^{j\omega}) = m$ a.e. Then the three properties 1), 2), and 3) presented in Theorem 2 are also equivalent if every phrase “class $H^2$” is replaced by the phrase “class $N^+$” in statements 2) and 3).

The proof of this theorem can be made in the same way as the proof of Theorem 2.

III. Conclusions

We have considered the linear discrete time systems with matrix-valued transfer functions of the Hardy class $H^2$ and more generally of the Smirnov class $N^+$, and obtained that the notion of minimum phase is equivalent to that of minimum-energy delay for these classes. This equivalence has been presented by means of the inner–outer factorization of transfer functions and the Parseval identity for $L^2$ class functions.

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High-Speed Delayed Multipath Two-Dimensional Digital Filtering Architecture

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Abstract—In this paper, a delayed multipath method for the realization of two-dimensional nonrecursive and recursive digital filters is presented. In this method, the two-dimensional transfer function polynomial is decomposed into a number of shorter transfer function polynomials in parallel.

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Each of these transfer function polynomials can be realized efficiently in terms of a number of processors. Consequently, high-speed computation can be obtained which can be applied to various digital-filtering applications. For a two-dimensional finite-impulse response digital filter of order $M_1$ and $M_2$, the maximum throughput can be $(M_2+1)(M_1+1)/2$ times of the conventional direct-form realization using one processor.

I. INTRODUCTION

High-speed digital filtering is important in many practical signal-processing applications. Generally speaking, high-speed filtering can be achieved by using high-speed digital component and/or by making use of concurrency in arithmetic computation. The latter can be achieved by utilizing the pipeline processing technique and/or parallel-processing technique.

Recently, a general decomposition theorem has been proposed [1] for the expansion of a general multidimensional rational function in terms of functions of one dimensional (1-D) only. Consequently, multidimensional digital filters can be implemented with great modularity and parallelism. Another method to the realization of two-dimensional (2-D) finite-impulse response (FIR) and infinite-impulse response (IIR) digital filters can be devised [2] using “lower-upper (LU) triangular decomposition” of the matrix coefficients of their two-dimensional polynomials. The method enjoys a number of attributes for VLSI implementation including high parallelism, modularity, and regularity. Moreover, parallel and high throughput structures can also be obtained [3] for the realization of 2-D digital filters using well-known transforms such as the discrete Fourier and Walsh–Hadamard.

Alternatively, instead of transforming the transfer function of a digital filter into another form with different coefficient value which facilitates high-speed realization as adopted in [1]–[3], the original transfer function can be used directly with the same coefficient values for realization. In fact, this is the approach characterized by the delayed $N$-path structure advanced recently in [4] and [5] for the realization of 1-D FIR and IIR digital filters. The resultant structure possesses high regularity, modularity, and parallelism. Moreover, the resultant throughput is $N^2$ times that of the conventional direct-form realization. In this contribution, the concept of the delayed $N$-path 1-D structure is formulated into a delayed multipath structure for 2-D FIR and IIR digital filters. This results in a significant improvement in the throughput rate of 2-D digital filters [7]. These are presented in Sections II and III. In Section IV, a comparison of the throughput and hardware requirements of the conventional direct-form realizations with those of the delayed multipath direct-form realizations of both FIR and IIR digital filters is given. Illustrative examples are also given in Section V.

II. DELAYED MULTIPATH FIR DIGITAL FILTER

Consider the transfer function of a 2-D FIR digital filter

$$H(z_1^1, z_2^1) = \sum_{m=0}^{M1} \sum_{n=0}^{M2} a(m,n) z_1^m z_2^n.$$  

(1)

In general, (1) can be decomposed as

$$H(z_1^1, z_2^1) = \sum_{j=0}^{N_2-1} z_2^{jL_2} \sum_{i=0}^{N_1-1} z_1^{i} A_{ij} (z_1^{-N_1}, z_2^{-1})$$  

(2)

In this paper, the conventional direct-form realization refers to the direct form realization in the form of a tapped delayed line (i.e., [2, figs. 1.12 and 1.15]) using one processor.
Fig. 1. A delayed direct-form 2-D FIR digital-filter structure suitable for multipath realization.

where

\[ A_{ij}(z^{-N1}, z^{-1}) = \sum_{k=0}^{L1-1} \sum_{l=0}^{L2-1} a(kN1 + i, l + jL2) z^{-kN1}z^{-l}. \quad (3) \]

In (2) and (3), \( N2 \) represents the number of \( z^{-jL2} (j = 0, 1, 2, \ldots, N2-1) \) branches from the input, \( L2 \) represents the incremental power of the \( z^{-jL2} \) branches, \( N1 \) represents the number of \( z^{-i} (i = 0, 1, 2, \ldots, N1-1) \) branches connected to the output of each \( z^{-jL2} \) branch, and \( L1 \) represents the number of \( z^{-kN1} \) terms \((k = 0, 1, 2, \ldots, L1-1) \) in \( A_{ij}(z^{-N1}, z^{-1}) \). Moreover, we have

\[ Mi + 1 = Ni \times Li \quad \text{for } i = 1, 2 \quad (4) \]

\[ 1 \leq N2 \leq M2 + 1 \quad (5) \]

and

\[ 1 < N1; \quad 1 < L1. \quad (6) \]

As seen from (2) and (3), the transfer function of a 2-D FIR digital filter is decomposed into \( N2N1 \) parallel transfer functions with each transfer function represented by a polynomial \( A_{ij}(z^{-N1}, z^{-1}) \) in \( z^{-N1} \) and \( z^{-1} \) together with a multiplication factor of \( z^{-jL2} \). Fig. 1 gives a representation of (2). In practice, each of the \( N2N1 \) transfer functions \( A_{ij}(z^{-N1}, z^{-1}) \) can be realized in terms of \( N1 \) identical parallel sections as shown in Fig. 2. In Fig. 2, the sampled input signal is connected sequentially by the input switch to the input of each of the \( N1 \) identical parallel sections in a round robin fashion at intervals of \( T1 \) (where \( z^{-1} = e^{-j\pi T1} \)) seconds. The output of each section is collected by the output switch which is in synchronization with the input switch. By incorporating Fig. 2 into Fig. 1, at any discrete time instant, the overall structure will give us a true realization of \( H(z^{-1}, z^{-1}) \) as given in (1).

### III. Delayed Multipath IIR Digital Filter

Consider the transfer function of a 2-D IIR digital filter

\[ H(z^{-1}, z^{-1}) = \sum_{m=0}^{M1} \sum_{n=0}^{M2} a(m, n) z^{-m}z^{-n}. \quad (7) \]

As seen from (2) and (3), the transfer function of a 2-D IIR digital filter is decomposed into \( N2N1 \) parallel transfer functions with each transfer function represented by a polynomial \( A_{ij}(z^{-N1}, z^{-1}) \) in \( z^{-N1} \) and \( z^{-1} \) together with a multiplication factor of \( z^{-jL2} \). Fig. 1 gives a representation of (2). In practice, each of the \( N2N1 \) transfer functions \( A_{ij}(z^{-N1}, z^{-1}) \) can be realized in terms of \( N1 \) identical parallel sections as shown in Fig. 2. In Fig. 2, the sampled input signal is connected sequentially by the input switch to the input of each of the \( N1 \) identical parallel sections in a round robin fashion at intervals of \( T1 \) (where \( z^{-1} = e^{-j\pi T1} \)) seconds. The output of each section is collected by the output switch which is in synchronization with the input switch. By incorporating Fig. 2 into Fig. 1, at any discrete time instant, the overall structure will give us a true realization of \( H(z^{-1}, z^{-1}) \) as given in (1).
where

\[ A_{ij}(z_{1}, z_{2}) = \sum_{k=0}^{L1-1} \sum_{l=0}^{L2-1} a(kN1 + i, l + jL2) z_{1}^{k} z_{2}^{l} \] (9)

\[ B_{ij}(z_{1}, z_{2}) = \sum_{k=0}^{L1-1} \sum_{l=0}^{L2-1} b(kN1 + i, l + jL2) z_{1}^{k} z_{2}^{l} \] (10)

and

\[ 1 < N1; \quad 1 < \frac{L1}{L1}. \] (16)

A 2-D IIR digital filter represented by (8) can be realized in a delayed direct-form structure shown in Fig. 3. In a manner similar to the FIR case, each of the transfer functions \( A_{ij}(z_{1}, z_{2}) \) and \( B_{ij}(z_{1}, z_{2}) \) of Fig. 3 can be realized, respectively, using \( N1 \) and \( N1 \) identical parallel sections as shown in Figs. 2 and 4. Consequently, the overall throughput rate is \( N2N1^2 \) or \( N2N1^2 \) (whichever is smaller) times faster than the conventional direct-form II realization (using one processor). The number of processors required for such a delayed multipath structure is \( N2N1^2 + N2N1^2 \). Assuming \( S1 \times S2 \) is the size of the input data to be processed, the memory requirements of each processor for storing coefficients and data (present and past input data) are, respectively, \( LL2 \) and \( [(L2-1)S1 + (L1-1)N1 + 1]/(N1) \) for the nonrecursive path or \( LL2 \) and \( [(L2-1)S1 + (L1-1)N1 + 1]/(N1) \) for the recursive path (see Table II).
Besides, the shared memory requirement for the delayed path is
\[(N2 - 1)L2S1 + N1\text{ or }((N2 - 1)L2S1 + N1)\text{ whichever is larger}.\]
In each processor, the input data to be stored has to be updated
(in a manner similar to the FIR case) at intervals of \(N1T1\) seconds for the nonrecursive path and \(N1T1\) seconds for the recursive path.

IV. COMPARISON OF THROUGHPUT AND HARDWARE REQUIREMENTS

Tables I and II summarize the throughput and hardware requirements of the conventional direct-form structures and the delayed multipath direct-form structures of 2-D FIR and IIR digital filters.

V. REALIZATION EXAMPLES

In this section, we shall illustrate the delayed multipath realization procedures of one 2-D FIR and one 2-D IIR digital filter examples. In general, the procedures apply to all other cases.

A. 2-D FIR Digital Filter

A 14\times14th-order 2-D FIR digital filter is chosen for illustration. From (1), we have

\[
H(z_1^{-1}, z_2^{-1}) = \sum_{m=0}^{14} \sum_{n=0}^{14} a(m, n) z_1^{-m} z_2^{-n}
\]

where \(M1 + 1 = 15\) and \(M2 + 1 = 15\). From (4) and (5), there exist four possible sets of values for \(N2\) and \(L2\); they are: (a) \(N2 = 1, L2 = 15\); (b) \(N2 = 3, L2 = 5\); (c) \(N2 = 5, L2 = 3\); and (d) \(N2 = 15, L2 = 1\). From (4) and (6), there exist two possible sets of values for \(N1\) and \(L1\); they are: (a) \(N1 = 3, L1 = 5\) and (b) \(N1 = 5, L1 = 3\). Altogether, there are eight possible combinations of \(N2, L2, N1,\) and \(L1\); hence, there are eight possible realizations. Table III gives a summary of the throughput and hardware requirements of these eight realizations. For illustration, the delayed multipath structure for \(N2 = 3, L2 = 5\) and \(N1 = 3, L2 = 5\) is shown in Fig. 5.

B. 2-D IIR Digital Filter

A 14\times14th-order 2-D IIR digital filter is chosen for illustration. From (7), we have

\[
H(z_1^{-1}, z_2^{-1}) = \sum_{m=0}^{14} \sum_{n=0}^{14} b(m, n) z_1^{-m} z_2^{-n}
\]

where \(M1 + 1 = 15\), \(M2 + 1 = 15\), \(N1 + 1 = 15\), and \(M2 + 1 = 15\). From (11), (13), and (15), there exist eight possible sets of values for \(N2, L2, N1,\) and \(L1\); they are: (a) \(N2 = 1, L2 = 15, N1 = 3,\) and \(L1 = 5\); (b) \(N2 = 1, L2 = 15, N1 = 5,\) and \(L1 = 3\); (c) \(N2 = 15, L2 = 1, N1 = 3,\) and \(L1 = 5\); (d) \(N2 = 15, L2 = 1, N1 = 5,\) and \(L1 = 3\); (e) \(N2 = 3, L2 = 5, N1 = 3,\) and \(L1 = 5\); (f) \(N2 = 3, L2 = 5, N1 = 5,\) and \(L1 = 3\); (g) \(N2 = 5, L2 = 3, N1 = 3,\) and \(L1 = 5\); and (h) \(N2 = 5, L2 = 3, N1 = 5,\) and \(L1 = 3\). Similarly, from (12), (14), and (16), there exist eight identical sets of
Fig. 5. The delayed multipath direct-form structure of a 14 x 14th-order 2-D FIR digital filter (N2 = N1 = 3, L2 = L1 = 5).

### TABLE III

**Throughput and Hardware Requirements of the Conventional Direct-Form and the Delayed Multipath Direct-Form of a 14 x 14th-Order 2-D FIR Digital-Filter Structure**

<table>
<thead>
<tr>
<th>Structure</th>
<th>Throughput Improvement</th>
<th>No. of Processors Required</th>
<th>Memory Requirement of Each Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>COEFFICIENT DATA STORAGE</td>
</tr>
<tr>
<td>Conventional Direct-Form</td>
<td>1</td>
<td>1</td>
<td>225</td>
</tr>
<tr>
<td>Delayed Multipath</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>9</td>
<td>9</td>
<td>75</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>25</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td>27</td>
<td>27</td>
<td>25</td>
</tr>
<tr>
<td>Direct-Form</td>
<td>75</td>
<td>75</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>45</td>
<td>45</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>125</td>
<td>125</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td>135</td>
<td>135</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>375</td>
<td>375</td>
<td>3</td>
</tr>
</tbody>
</table>

Values for N2, L2, N1, and L1. The throughput and hardware requirements of these eight realizations are summarized in Table IV. For illustration, the delayed multipath structure for N2 = N2 = 3, L2 = L2 = 5, N1 = N1 = 3, and L1 = L1 = 5 is shown in Fig. 6.

### VI. Concluding Remarks

In this paper, a delayed multipath method for the realization of 2-D FIR and IIR digital filters has been presented. The method is flexible in the sense that the rate of throughput improvement and the hardware complexity depend on the choices of values for...
Fig. 6. The delayed multipath direct-form structure of a $14 \times 14$-order 2-D IIR digital filter ($N_2 = N_2 = N_1 = N_1 = 1, L_2 = L_2 = L_1 = L_1 = 5$).

### Table IV

<table>
<thead>
<tr>
<th>Structure</th>
<th>Throughput Improvement</th>
<th>No. of Processors Required</th>
<th>Memory Requirement of Each Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Coefficient Storage</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Data Storage</td>
</tr>
<tr>
<td>Conventional Direct-Form II</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$N_2 = N_2 = 1$</td>
<td>$L_2 = L_2 = 1$ = 14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$N_1 = N_1 = 3$</td>
<td>$L_1 = L_1 = 5$</td>
<td>9</td>
<td>18</td>
</tr>
<tr>
<td>$N_2 = N_2 = 1$</td>
<td>$L_2 = L_2 = 15$</td>
<td>25</td>
<td>50</td>
</tr>
<tr>
<td>$N_1 = N_1 = 5$</td>
<td>$L_1 = L_1 = 3$</td>
<td>5</td>
<td>25</td>
</tr>
<tr>
<td>$N_2 = N_2 = 3$</td>
<td>$L_2 = L_2 = 5$</td>
<td>45</td>
<td>90</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Delayed Multipath Direct-Form</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_2 = N_2 = 3$</td>
<td>$L_2 = L_2 = 5$</td>
<td>75</td>
<td>150</td>
</tr>
<tr>
<td>$N_1 = N_1 = 5$</td>
<td>$L_1 = L_1 = 3$</td>
<td>25</td>
<td>54</td>
</tr>
<tr>
<td>$N_2 = N_2 = 5$</td>
<td>$L_2 = L_2 = 5$</td>
<td>27</td>
<td>54</td>
</tr>
</tbody>
</table>

| $N_1 = N_1 = 3$ | $L_1 = L_1 = 5$   | 95                       | 15                                  |
| $N_2 = N_2 = 3$ | $L_2 = L_2 = 3$  | 25                       | 35                                  |
| $N_1 = N_1 = 5$ | $L_1 = L_1 = 3$   | 225                      | 35                                  |
| $N_2 = N_2 = 5$ | $L_2 = L_2 = 3$  | 275                      | 35                                  |
| $N_1 = N_1 = 3$ | $L_1 = L_1 = 5$   | 750                      | 35                                  |
| $N_2 = N_2 = 3$ | $L_2 = L_2 = 3$  | 90                       | 15                                  |
| $N_1 = N_1 = 5$ | $L_1 = L_1 = 3$   | 250                      | 95                                  |
| $N_2 = N_2 = 5$ | $L_2 = L_2 = 3$  | 375                      | 250                                 |

Note: The throughput and hardware requirements are calculated for processing input data of $768 \times 768$. The memory requirements include coefficient storage and data storage.
roundoff error analysis of the 2-D delayed multipath structure the first-order McClellan transformation so as to map the cutoff
provided its
Institute of Technology, New Delhi 110016 India.

and its comparisons with other implementation structures are frequency of the 1-D filter onto a circular contour in a 2-D
obtained by this analytic technique are nearly identical to those obtained
method presented can also be applied to individual section using the McClellan transformation [1]. Various techniques [1]-[6] --

Further work on 2-D and 3-D delayed multipath realization methods can be found in [8] and [9]. The finite word-length
roundoff error analysis of the 2-D delayed multipath structure and its comparisons with other implementation structures are
topics that are currently under investigation.

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Design of Elliptically Symmetric Two-Dimensional
FIR Filters Using the McClellan Transformation

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Abstract—An analytic technique for choosing the coefficients of the
first-order McClellan transformation for the design of elliptically symmet-
tric two-dimensional FIR filters is described. It is found that the results
obtained by this analytic technique are nearly identical to those obtained
by an optimization procedure reported earlier. The number of multiplica-
tions per output sample required to implement these filters is shown to be
small.

I. INTRODUCTION

Elliptically symmetric two-dimensional (2-D) filters are useful
in many situations. For example, there may be compelling rea-
sions to use different sampling rates in the two spatial directions.
In such cases, the design of filters with a circularly symmetric
response reduces to the design of filters with elliptic symmetry.

One of the most powerful techniques for designing 2-D FIR
filters is the transformation of a one-dimensional (1-D) FIR filter
using the McClellan transformation [1]. Various techniques [1]-[6]
have been proposed to determine the coefficients of the McClel-
lan transformation to approximate a given passband boundary of
a 2-D filter with piecewise-constant frequency response. Re-
cently, a simple analytic technique to choose the coefficients of
the first-order McClellan transformation so as to map the cutoff
frequency of the 1-D filter onto a circular contour in a 2-D
frequency plane with a high degree of accuracy was proposed [7].
Here, we extend this technique to 2-D filters with elliptic symme-
try and obtain some interesting results. From the computations
of several examples, it is found, for a first-order transformation
and for a specific error criterion, that the results obtained by the
analytic technique are nearly identical to those obtained by using
the optimization procedure of [2]. The number of multiplications
required to implement these filters is shown to be quite small.

II. THE TECHNIQUE

The passband boundary of a low-pass elliptic symmetric
filter is described by

\[
\left( \frac{\omega_1}{\omega_{1c}} \right)^2 + \left( \frac{\omega_2}{\omega_{2c}} \right)^2 = 1
\]

(1)

where \(\omega_1\) and \(\omega_2\) are the frequency variables of the 2-D filters. The variables \(\omega_{1c}\) and \(\omega_{2c}\) are the passband edge frequencies on
the \(\omega_1\)-axis and the \(\omega_2\)-axis, respectively. (We shall assume \(\omega_{2c} > \omega_{1c}\); the case \(\omega_{2c} < \omega_{1c}\) is exactly analogous.) The first-order
McClellan transformation is given by

\[
\cos \omega = F(\omega_1, \omega_2)
\]

(2)

When expressed in sine functions, (2) reduces to

\[
\sin^2 \left( \frac{\omega}{2} \right) = F(\omega_1, \omega_2) = t_{00} + t_{10} \sin^2 (\omega_1/2) + t_{01} \sin^2 (\omega_2/2)
+ t_{11} \sin^2 \left( \frac{\omega_1}{\omega_{1c}} \right) \sin^2 \left( \frac{\omega_2}{\omega_{2c}} \right)
\]

(3)

where \(\omega\) is the frequency variable of the 1-D filters, in rad/s. We
choose the coefficients \(t_{pq}\) using the following considerations.
The point \(\omega = 0\) maps onto \((0,0,0,0,0)\), and the cutoff
frequency of the 1-D prototype filter, maps onto the points
\((\omega_{1c},0,0,0,0)\), \((0,\omega_{2c},0,0,0)\), and \((\omega_{1c}/\sqrt{2},\omega_{2c}/\sqrt{2})\) in the \((\omega_1,\omega_2)\)-plane. This gives
\(t_{00} = 0\), \(t_{10} = a/b_1\), \(t_{01} = a/b_2\), and \(t_{11} = a/b_2 + c_1 - c_2\),
where

\[
a = \sin^2 \left( \frac{\omega_1}{2} \right)
\]

(4a)

\[
b_i = \sin^2 \left( \frac{\omega_{ic}}{2} \right), \quad i = 1,2
\]

(4b)

and

\[
c_i = \sin^2 \left( \frac{\omega_{ic}/\sqrt{2}}{2} \right), \quad i = 1,2
\]

(4c)

Finally, we choose \(a\), i.e., \(\omega_c\), such that

\[0 < F(\omega_1, \omega_2) < 1\]

(5)