in more diffraction and the beam expanded to 3-6 times over 5mm, as shown in Fig. 2. From eqn. 3 it is clear than a decrease in the beam size will result in an increase in the peak power requirements to observe self-focusing. Fig. 2 shows the spatial soliton occurring at an increased peak power level of 1.07 kW.

AlGaAs system has several advantages over other materials for the realization of spatial soliton based devices, namely; low losses, both linear and nonlinear, high nonlinear refractive coefficient and a well understood fabrication technology.

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References

DELAYED N-PATH STRUCTURE FOR HIGH SPEED ADAPTIVE FIR DIGITAL FILTERING
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Indexing terms: Filters, Adaptive filters, Digital filters, Modelling, Algorithms

A structure and its algorithm for high speed adaptive FIR digital filtering based on the delayed N-path concept is presented. Using N² processors, the throughput rate of the proposed filter can be N³ times faster than that of the same filter realised directly using one such processor.

Introduction: There exist various adaptive filter structures and algorithms [1, 2]. However, high speed structures and algorithms for adaptive digital filtering have yet to be developed for high speed processing of signals containing significant high frequency components. Block digital filtering [3, 4] is a well known technique for increasing the throughput rate which can be realised using L parallel processors with a throughput improvement of a factor of L (where L is the input and output

Fig. 1 Time averaged mode profiles for input beam with 1/e² radius of 20 µm as function of input power
a Input beam profile
b Low power (~ 5 W) output showing effects of diffraction
c Output profile for peak power of 760 W

Conclusions: We have carried out preliminary experiments on spatial optical soliton propagation in AlGaAs semiconductor waveguides. At low power levels the beam was observed to diffract as it propagated, while at higher input power levels the effects of the negative nonlinearity gave rise to self-focusing and the collapse of the input to form a spatial soliton. The
block length). The same improvement in throughput rate can also be obtained in block adaptive digital filters (BADFs) [5, 6]. The principle of block and block adaptive digital filters is based on parallel processing in which each of the L parallel processors computes one output based on one block of L consecutive inputs. Delayed N-path digital filtering is a new technique for high speed digital filtering using $N^2$ digital signal processors (DSPs) with a maximum throughput rate improvement of a factor of $N^2$ [7]. For linear phase FIR digital filters, the corresponding maximum throughput rate improvement is $2N^2$ [8] and can be further increased using the systolic array structure [9] by speeding up its clock cycle.

It was suggested [8, 9] that high speed adaptive digital filtering can be achieved using the concept of the delayed N-path structure. In this Letter, a structure and its algorithm for high speed adaptive FIR digital filters called delayed N-path adaptive FIR (DNAFIR) digital filters is presented (for $N \geq 2$). The proposed DNAFIR digital filter (as seen in Fig. 1 for system modelling) has a number of different features as compared to a block adaptive digital filter (BADF). First, a DNAFIR digital filter is a single-output filter (as compared to an L-output filter in a BADF). Secondly, the formulation of a DNAFIR digital filter is based on systematic transfer function decomposition (see eqns. 2–4) (as compared with having L original transfer functions in parallel form in a BADF). In a DNAFIR digital filter, its original transfer function is first decomposed into N delayed subfilters (each of about 1/N of the length of the original transfer function) which can then be realised directly in the form of N parallel paths. Each of these N parallel paths can further be realised directly by N parallel DSPs. Each of these N parallel DSPs in a path is allowed to operate at a sampling rate of N times slower than that of the input signal for realising an identical set of variable coefficient subfilters and the associated adaptive algorithm.

Thirdly, the number of coefficients to be updated in each of the $N^2$ DSPs of a DNAFIR digital filter is about 1/N times that of the total number of coefficients M (as compared to M coefficients in each of the L parallel paths of a BADF). On combining the second and third features of a DNAFIR digital filter, given $N^2$ DSPs of a certain maximum speed, the maximum speed of a DNAFIR digital filter can be $N^2$ times (as compared to L times using L DSPs in a BADF) that of the same adaptive FIR digital filter realised directly using one such DSP.

**DNAFIR digital filter**: Consider the transfer function of an adaptive FIR digital filter at a discrete time k as

$$H(z^{-1}) = \sum_{m=0}^{M-1} h(m)z^{-m}$$

(1)

Egn. 1 can be decomposed into the following form for delayed N-path realisation:

$$H(z^{-1}) = \sum_{k=0}^{k-1} H_k(z^{-1})$$

(2)

where

$$H_k(z^{-1}) = \sum_{j=0}^{L_k} h(j/N + 0)z^{-jN}$$

(3)

in which

$$L_i = [M/N]^i$$

for $i = 0, 1, \ldots, J - 1$$

(4a)

and

$$L_i = [M/N]^i + 1$$

for $i = J, J + 1, \ldots, N - 1$$

(4b)

and

$$J = M \mod N$$

(4c)

[M/N]$^i$ of eqns. 4a and 4b represents the largest integer smaller than or equal to $M/N$. It should be noted that even though the transfer function as expressed in eqn. 2 is of identical form to that of the well known polyphase filter [10]. Eqn. 2 can be used to realise a DNAFIR digital filter consisting of $N^2$ processors (or subfilters) which is different from that of $N$ subfilters in a polyphase filter. This DNAFIR digital filter can be used in adaptive system modelling as shown in Fig. 1. If we denote the input signal as $x(k)$ and the output signal as $y(k)$, we have the following input-output relationship:

$$y(k) = \sum_{i=0}^{k-1} y_i(k)$$

$$= \sum_{i=0}^{k-1} \sum_{j=0}^{L_i} h(i/N + j)z^{-jN} - \sum_{i=0}^{k-1} \delta_h(jN + \bar{i})$$

(5)

where $\delta_h(k)$ is the output of the ith path as shown in Fig. 1. Let $d(k)$ represent the desired output at discrete time k; the squared output error at discrete time k is defined as

$$e(k) = (d(k) - y(k))^2$$

(6)

Define the change of a coefficient, $\delta h_i(jN + \bar{i})$ as

$$\delta h_i(x(N + \bar{i})) = -\mu \delta h_i(x(N + \bar{i}))$$

(7)

where $\mu$ is a convergence parameter. From eqns. 5–7, we obtain

$$h_{k+1}(x(N + \bar{i})) = h_k(x(N + \bar{i}) + 2\mu e(k)x(N + \bar{i}))$$

(8)

for $i = 0, 1, \ldots, N - 1$ and $j = 0, 1, \ldots, L_i$.

**Simulation results**: For illustration, the results of two typical examples are presented here. In both cases, software generated white noise was used for the input $x(k)$ of Fig. 1. A 14th order FIR digital filter of transfer function

$$H(z^{-1}) = 1 + 2z^{-1} + 3z^{-2} + 4z^{-3} + 5z^{-4} + 6z^{-5} + 7z^{-6} + 8z^{-7} + 9z^{-8} + 10z^{-9}$$

was modelled by a 14th order delayed four-path adaptive FIR digital filter structure (with $M = 15$ and $N = 4$). With $\mu$ set to 0.1, the output error curve is shown in Fig. 2. After 1000 iterations, i.e. 250 iterations for each path, the average squared output error over 20 iterations fell below 10$^{-7}$. A 6th order FIR digital filter of transfer function

$$H(z^{-1}) = (1 - 7 + 2z^{-1} + 3z^{-2} + 3z^{-3} - 3z^{-4})$$

was modelled by a 6th order delayed four-path adaptive FIR digital filter structure (with $M = 8$ and $N = 4$). With $\mu$ set to 0.002, the output error curve is shown in Fig. 3. After 1000 iterations, the average squared output error over 20 iterations fell below 10$^{-7}$. A 2nd order FIR digital filter of transfer function

$$H(z^{-1}) = (1 - 0.9z^{-1})$$

Fig. 1 System modelling using delayed N-path adaptive FIR digital filter structure

**ELECTRONICS LETTERS** 24th September 1992 Vol. 28 No. 20 1881
was modelled by a 26th order delayed three-path adaptive FIR digital filter structure (with $M = 27$ and $N = 3$). With $\mu$ set to 0.08, the output error curve is shown in Fig. 3. After 1700 iterations, i.e. 500 iterations for each path, the average squared output error over 30 iterations fell below $10^{-5}$.

Fig. 2 Output error curve of 14th order delayed four-path adaptive FIR digital filter in system modelling

Conclusions: In this Letter, the structure of a delay $N$-path adaptive FIR digital filter has been presented. Based on this structure, an adaptive algorithm was developed which is applicable to any arbitrary $N$-path realisation (for $N \geq 2$). The DNAFIR digital filter structure can be realised using $N^2$ DSPs with a maximum throughput rate of $N^2$ times that of the same adaptive FIR digital filter realised directly using one such DSP. This kind of DNAFIR digital filter is extremely suitable for high speed adaptive filtering in which the upper processing speed limit imposed by the most advanced digital signal processor chip can be increased by a factor of $N$ times (as a result of $N$ slowed-down processing speeds in all of the $N$ ‘parallel’ $N$ DSP blocks). This is in addition to a speed improvement of $N$ times due to parallel decomposition of the original transfer function.

Fig. 3 Output error curve of 26th order delayed three-path adaptive FIR digital filter in system modelling

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References

THREE-STEP PIN ASSIGNMENT ALGORITHM FOR BUILDING BLOCK LAYOUT

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Indexing terms: Algorithms, Computer-aided design, Circuit design

A new pin assignment algorithm is proposed which can be used in floorplanning and building block layout to minimise the total wiring length and channel area while satisfying the minimum distance constraint among pin positions on the block boundary. This algorithm can be used in floorplanning in which block shapes are iteratively modified by the channel density obtained as a result of global routing. The proposed pin assignment algorithm occurs in three steps: approximate pin assignment, global routing and detailed pin assignment. Experimental results were obtained using MCNC placement and floorplanning benchmark examples.

Introduction: In building block layout, the main objective is to determine the shapes and positions of blocks so that the total layout area and/or the total interconnection length is minimal. Because of the complexity of the problem, it is usually divided into four steps: floorplanning, pin assignment, global routing and detailed routing. The pin assignment step determines the pin positions on the boundaries of building blocks. Judicious assignment of these pins can improve the routing area and the interconnection delay by reducing wire length, crossovers and wire congestion.

Various approaches for pin assignment in the building block layout have been proposed such as the concentric circle mapping method [1], nine zone method [2], and topological pin assignment method [3]. However, because these approaches perform the pin assignment on a block by block basis, the resultant quality is very sensitive to the processing order of blocks. In Reference 4, where a physical analogy was used for the pin assignment problem, the pin positions are approximate because blocks are mapped to circles. Cong [5] combines the pin assignment step with global routing. However, the pin positions, once assigned to an edge of a block periphery, cannot be moved to another block edge for minimising the wiring length, thereby leading to suboptimal results.

ELECTRONICS LETTERS 24th September 1992 Vol. 28 No. 20