A Multi-Output Second-Order Digital Filter Structure for VLSI Implementation

HON KEUNG KWAN

Abstract — A multi-output second-order digital filter structure without zero-input and constant-input oscillations is presented. It could be used for the realization of low-pass, high-pass, band-pass, and band-stop Butterworth, Chebyshev, and elliptic digital filters, and all-pass digital filters. The overall structure consists of two delays, three multipliers, and nine adders, which could be adopted for VLSI implementation.

I. INTRODUCTION

The commercial availability of second-order digital filters in chip form enables many potential users to employ them in various applications without going through the process of either software or hardware implementation [1]. In this contribution, we present a multi-output second-order digital filter structure which is derived from the passive design method [2], [3] which we have developed previously. The filter structure can be used for the realization of all frequency-band Butterworth, Chebyshev, and elliptic digital filters and can be adapted for VLSI implementation.

II. TYPES OF TRANSFER FUNCTIONS

As seen from the Filter Design Handbook [4], a low-pass (LP) Butterworth or Chebyshev filter consists of

$$T_{LP}(s) = \frac{1}{s - \lambda_i}$$

for an odd-order filter

and combinations of

$$T_{LP}(s) = \frac{1}{s^2 - 2\lambda_0 s + \gamma_0}$$

for odd- and even-order filters.

Applying the bilinear transformation [5]

$$s = \frac{2}{T} \frac{1 - z^{-1}}{1 + z^{-1}}$$

together with either the digital or analog frequency transformation [5] to (1) and (2), low-pass, high-pass (HP), band-pass (BP), and band-stop (BS) second-order digital transfer functions can be expressed as

$$T_{LP}(z^{-1}) = a(1 + z^{-1})^2/D(z^{-1})$$

$$T_{HP}(z^{-1}) = a(1 - z^{-1})^2/D(z^{-1})$$

$$T_{BP}(z^{-1}) = a(1 - z^{-2})^2/D(z^{-1})$$

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Fig. 1. A digital two-port.

Fig. 2. A multi-output second-order digital filter ($B = 1$ for $v_{AP}(k)$; MT: magnitude truncation).

$$T_{BS}(z^{-1}) = a(1 + a_1 z^{-1} + z^{-2}) / D(z^{-1})$$  (8)

where

$$D(z^{-1}) = 1 + b_1 z^{-1} + b_2 z^{-2}. \quad (9)$$

Similarly, from (3), the four corresponding second-order digital transfer functions can be expressed as

$$T'(z^{-1}) = a(1 + a_1 z^{-1} + z^{-2}) / D(z^{-1}). \quad (10)$$

Finally, a second-order all-pass (AP) digital transfer function can be expressed as

$$T_{AP}(z^{-1}) = (b_2 + b_1 z^{-1} + z^{-2}) / D(z^{-1}) \quad (11)$$

III. MULTI-OUTPUT SECOND-ORDER DIGITAL FILTER

A multi-output second-order digital filter which is capable of realizing all the digital transfer functions as given in (5)-(11) can be obtained using the passive two-port approach as presented in [3]. Using the two-port, as shown in Fig. 1, a multi-output second-order digital filter, consisting of two delays, three multipliers and, nine adders can be obtained, as shown in Fig. 2. The actual digital transfer function of each of the filters can be obtained by taking the $z$-transform of the output discrete-time signal over the $z$-transform of the input discrete-time signal. Consequently, they could be expressed as

$$T_{LP}(z^{-1}) = \left[ v_{LP}(k) \right] Z[u(k)]$$

$$= (1 - \alpha_2)(1 + z^{-1})^2 / D(z^{-1}) \quad (12)$$

$$T_{HP}(z^{-1}) = \left[ v_{HP}(k) \right] Z[u(k)]$$

$$= (1 + \alpha_1)(1 - z^{-1})^2 / D(z^{-1}) \quad (13)$$

$$T_{BP}(z^{-1}) = \left[ v_{BP}(k) \right] Z[u(k)]$$

$$= -(1 - z^{-2}) / D(z^{-1}) \quad (14)$$

$$T_{BS}(z^{-1}) = \left[ v_{BS}(k) \right] Z[u(k)]$$

$$= T'(z^{-1}) \quad (15)$$

$$= Z[v'(k)] Z[u(k)]$$

$$= \{1 + (2[\beta(1 - \alpha_2) - (1 + \alpha_1)] / D(z^{-1}) \}

Finally, a second-order all-pass (AP) digital transfer function can be expressed as

$$T_{AP}(z^{-1}) = \left[ v_{AP}(k) \right] Z[u(k)]$$

$$= (1 + \alpha_1 - \alpha_2) - (\alpha_1 + \alpha_2) z^{-1} + z^{-2} / D(z^{-1}) \quad (16)$$

where

$$D(z^{-1}) = 1 - (\alpha_1 + \alpha_2) z^{-1} + (1 + \alpha_1 - \alpha_2) z^{-2}. \quad (17)$$

IV. CONCLUSIONS

A multi-output second-order digital filter structure has been presented. The structure is flexible and consists of only two delays, three multipliers, and nine adders. With magnitude truncations at the outputs of the two-port, both zero-input and constant-input oscillations can be eliminated in this filter [2], [3]. Moreover, the coefficients of a digital transfer function can be obtained by matching with the coefficients of the corresponding analog transfer function obtained from the Filter Design Handbook [4]. Consequently, the filter structure is quite suitable for VLSI implementation.

REFERENCES


