Systolic Array Implementation of $H(z^{-1})$

$$H(z^{-1}) = \frac{a_0 + a_1 z^{-N} + a_2 z^{-2N}}{1 + b_1 z^{-N} + b_2 z^{-2N}}, \quad \text{for } N \geq 2$$

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Abstract—A novel systolic array for the implementation of a second-order IIR transfer function expressed in terms of $z^{-N}$ is presented. The array is suitable for any value of $N$ greater than or equal to two. The major advantages of this systolic array include nearest neighbor interconnection and only three identical basic cells are required.

I. INTRODUCTION

In this paper, we consider the problem of how a second-order infinite impulse response (IIR) $N$-path digital element can be implemented systolically such that a delayed multipath IIR digital filter structure [1] can be realized in terms of a number of these second-order arrays.

II. SYSTOLIC REALIZATION

Consider a second-order IIR $N$-path digital element as defined by

$$H(z^{-1}) = \frac{a_0 + a_1 z^{-N} + a_2 z^{-2N}}{1 + b_1 z^{-N} + b_2 z^{-2N}}, \quad \text{for } N \geq 2. \quad (1)$$

This IIR $N$-path digital element can be realized systolically using one type of basic cell, as defined in Fig. 1. The basic cell consists of two multipliers and two adders. The two multipliers can be arranged to operate in parallel and the two adders can be arranged to operate in sequence. Assuming $T_m$ and $T_a$ are, respectively, the times required for a real multiplication and a real addition. The minimum cycle time of the basic cell is $T_{min} = T_m + 2T_a$. The purpose of realizing (1), three basic cells are required to be interconnected, as shown in Fig. 2. For operations, the basic cells are first initialized to zero state and the input data $x(n)$ are passed into the array at the top left-hand corner of the resultant array shown in Fig. 2. The output data are then obtained once per operation cycle from the bottom left-hand corner of the array. For illustration, the status of the array at $n = 0, 1, 7,$ and $8$ are shown in Fig. 3 for $N = 3$.

III. CONCLUSIONS

A systolic array for the realization of a second-order IIR $N$-path digital element has been presented. The resultant array is regular, is characterized by nearest neighbor interconnection, and consists of only one type of basic cell. Under finite wordlength arithmetic operations, quantization can be carried out by applying magnitude truncation to $y(n)$ located at the bottom left-hand corner of Fig. 2 before it is allowed to feedback to the leftmost cell. In so doing, limit-cycle oscillations can mostly be eliminated [2]. The proposed array is useful for the systolic or high-speed implementation of any digital system consisting of one or more such IIR $N$-path digital elements. One such system is the delayed multipath IIR digital filter structure shown in Fig. 5 of [1]; details will appear later [3].

REFERENCES

